Abstract of the Disclosure

A bypass system for a data cache has two ports to the data cache, registers for multiple data entries, a bus connection for accepting read and write operations to the cache, and address matching and switching logic. The system is characterized in that write operations that hit in the data cache are stored as elements in the bypass structure before the data is written to the data cache, and read operations use the address matching logic to search the elements of the bypass structure to identify and use any one or more of the entries representing data more recent than that stored in the data cache memory array, such that a subsequent write operation may free a memory port for a write stored in the bypass structure to be written to the data cache memory array. In a preferred embodiment there are six entries in the bypass system, and stalls are eliminated.